WHAT IS CLAIMED IS:

1. A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test mode, where N > 1 and each domain has a plurality of scan cells, said method comprising the steps of:

(a) generating and loading N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during the shift operation;

(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains during the capture operation;

(c) compacting N output responses of all said scan cells to signatures during the compact operation; and

(d) repeating the steps of (a)-(c) until a predetermined limiting criteria is reached, wherein (a) and (c) occur substantially concurrently.

2. The method of claim 1, wherein each said capture clock is programmable to contain one or more clock pulses for performing said shift/compact and capture operations on all said scan cells within one said clock domain; wherein said clock domain is solely controlled by said capture clock; and said capture clock can be either generated

internally or controlled externally, and can operate either at its rated clock speed (at-speed) or at a selected clock speed.

3. The method of claim 1, further comprising providing N scan enable (SE) signals each within one said clock domain; wherein said SE signals are used to switch operations from shift/compact to capture, and vice versa; and further said SE signals can be generated internally or controlled externally, and are operated either at the rated clock speeds (at-speed) or at selected clock speeds.

4. The method of claim 3, wherein said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive said N scan enable (SE) signals; wherein said GSE signal is operated at a selected reduced clock speed.

5. The method of claim 1, wherein said generating and loading N pseudorandom stimuli further comprises operating all capture clocks at selected clock speeds or at the same clock speed, and when operated at the same clock speed, all said capture clocks are skewed so that at any given time only scan cells within one said clock domain are changing states to reduce power consumption.

6. The method of claim 1, further comprising the step of comparing said signatures with their expected signatures for error indication, after said predetermined limiting criteria is reached; wherein said step of comparing said signatures with their expected signatures further comprises comparing said signatures inside said integrated circuit or circuit assembly or shifting out said signatures for comparison in an ATE.

7. The method of claim 1, wherein said generating and loading N pseudorandom stimuli further comprises using a plurality of pseudorandom pattern generators (PRPGs) and phase shifters.

8. The method of claim 7, wherein each said pseudorandom pattern generator (PRPG) further comprises using a finite-state machine to automatically generate a number of test patterns; wherein said test patterns are applied through a phase shifter to a plurality of clock domains.

9. The method of claim 7, wherein each said phase shifter further comprises using a combinational logic network to decompress said test patterns to said pseudorandom stimuli.

10. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises performing said capture operation concurrently on a plurality of clock domains which do not have any logic block crossing each other.

11. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises applying said capture clocks in a selected order for detecting or locating additional faults in said integrated circuit or circuit assembly.

12. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises applying another ordered sequence of capture clocks selectively longer or shorter than said ordered sequence of capture clocks for detecting or locating additional faults in said integrated circuit or circuit assembly.

13. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises disabling one or more capture clocks to facilitate fault diagnosis.

14. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises selectively operating said capture clock at a selected

clock speed for detecting or locating stuck-at faults within the clock domain controlled by said capture clock.

15. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises selectively operating said capture clock at its rated clock speed for detecting or locating delay faults within the clock domain controlled by said capture clock.

16. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises selectively reducing said capture clock speed to the level where delay faults associated with all multiple-cycle paths of equal cycle latency within the clock domain are tested at a predetermined rated clock speed.

17. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises selectively operating two said capture clocks at selected clock speeds for detecting or locating stuck-at faults crossing two said clock domains.

18. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises selectively adjusting the relative clock delay of two said capture clocks operating at selected clock speeds for

detecting or locating delay faults crossing two said clock domains.

19. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises selectively adjusting the relative clock delay of two said capture clocks to the level where delay faults associated with all multiple-cycle paths of equal cycle latency crossing two said clock domains are tested at a predetermined rated clock speed.

20. The method of claim 1, wherein said applying an ordered sequence of capture clocks further comprises controlling the relative clock delay between any two adjacent capture clocks internally or external to said integrated circuit or circuit assembly.

21. The method of claim 1, wherein said compacting N output responses further comprises using a plurality of space compactors and multiple-input signature registers (MISRs).

22. The method of claim 21, wherein each said space compactor further comprises using a combinational logic network to compress said output responses to compressed output responses.

23. The method of claim 21, wherein each said multiple-input signature register (MISR) further comprises using a finite-state machine to compact said compressed output responses to a signature; said MISR compacts said output responses through a space compactor to said signature.

24. The method of claim 1, further comprising using a PRPG-MISR pair to test faults within a plurality of clock domains when all capture clocks of said a plurality of clock domains operate at the same clock speed; all said capture clocks are skewed so as to eliminate races and timing violation during each shift, capture, or compact operation.

25. The method of claim 24, wherein said PRPG-MISR pair further comprises a PRPG, an optional phase shifter, an optional space compactor, a MISR, and a comparator.

26. The method of claim 25, wherein said PRPG-MISR pair further comprises connecting said PRPG to the first-arrived capture clock and connecting said MISR to the last-arrived capture clock within said a plurality of clock domains.

27. The method of claim 1, wherein said compacting N output responses further comprises selectively comparing

said N output responses directly with their expected output responses and indicating errors immediately using a compare operation.

28. The method of claim 1, wherein said scan cells are multiplexed D flip-flops or level sensitive latches, and further wherein said integrated circuit or circuit assembly under test is a full-scan or partial-scan design.

29. The method of claim 1, wherein said faults further comprise stuck-at faults and delay faults; wherein said stuck-at faults further comprises other stuck-type faults, such as open and bridging faults, and wherein said delay faults further comprise other non-stuck-type delay faults, such as transition (gate-delay), multiple-cycle delay, and path-delay faults.

30. An apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test mode, where N > 1 and each domain has a plurality of scan cells, said apparatus comprising:

(a) means for generating and loading N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during the shift operation;

(b) means for applying an ordered sequence of capture clocks to all said scan cells within said N clock domains during the capture operation;

(c) means for compacting N output responses of all said scan cells to signatures during the compact operation; and

(d) means for repeating the steps of (a)-(c) until a predetermined limiting criteria is reached, wherein (a) and (c) occur substantially concurrently.

31. The apparatus of claim 30, wherein said means of (a)-(d) are placed inside or external to said integrated circuit or circuit assembly.

32. A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test mode, where N > 1 and each domain has a plurality of scan cells, said method comprising the steps of:

(a) shifting in N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during the shift-in operation;

(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains during the capture operation; and

(c) shifting out N output responses of all said scan cells for analysis during the shift-out operation.

33. The method of claim 32, further comprising providing N scan enable (SE) signals each within one said clock domain; wherein said SE signals are used to switch operations from shift/compact to capture, and vice versa; and further said SE signals can be generated internally or controlled externally, and are operated either at the rated clock speeds (at-speed) or at selected clock speeds.

34. The method of claim 33, wherein said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive said N scan enable (SE) signals; wherein said GSE signal is operated at a selected reduced clock speed.

35. The method of claim 32, wherein said applying an ordered sequence of capture clocks further comprises any means for generating the ordered capture sequence; wherein said ordered capture sequence does not include any shift clock pulses during said capture operation.

36. A computer-aided design (CAD) system for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in

self-test mode, where N > 1 and each domain has a plurality of scan cells, said CAD system comprising the computer-implemented steps of:

(a) compiling the HDL code or netlist that represents said integrated circuit or circuit assembly in physical form into a design database;

(b) performing self-test rule check for checking whether said design database contains any multiple-capture self-test rule violations;

(c) performing self-test rule repair until all said multiple-capture self-test rule violations have been fixed;

(d) performing multiple-capture self-test synthesis for generating a self-test HDL code or netlist; and

(e) generating HDL test benches and ATE test programs for verifying the correctness of said self-test HDL code or netlist.

37. The CAD system of claim 36, wherein said steps of (a)-(e) accept user-supplied self-test control information and report the results and errors, if any.

38. The CAD system of claim 36, wherein said performing self-test rule check further comprises determining the number of clock domains and capture clocks required for self-test, the clock domains to be tested concurrently, the ordered sequence of capture clocks to be

applied for self-test, and the capture clocks to be operated at the rated clock speeds or at selected clock speeds.

39. The CAD system of claim 36, wherein said performing multiple-capture self-test synthesis further comprises the hierarchical computer-implemented steps of:

(a) synthesizing a plurality of PRPG-MISR pairs one at a time for each individual clock domain or combined clock domains, wherein each said PRPG-MISR pair further comprises a PRPG, an optional phase shifter, an optional space compactor, a MISR, and a comparator;

(b) synthesizing a central self-test controller which includes an error indicator; and

(c) stitching said central self-test controller together with said PRPG-MISR pairs.

40. The CAD system of claim 39, wherein said synthesizing a plurality of PRPG-MISR pairs domain-by-domain further comprises inserting spare scan cells into selected clock domains.

41. The CAD system of claim 36, wherein said performing multiple-capture self-test synthesis realizes said apparatus of claim 30 using said method of claim 1.

42. The CAD system of claim 36, wherein said generating HDL test benches and ATE test programs further comprises the steps of transforming said design database into an equivalent combinational circuit model based on said ordered sequence of capture clocks, and performing combinational fault simulation to compute the circuit's output responses, signatures, and fault coverage.

43. A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test mode, where N > 1 and each domain has a plurality of scan cells, said method comprising the steps of:

(a) generating and loading N predetermined stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during the shift operation;

(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains where one or more capture clocks must contain two or more clock pulses during the capture operation;

(c) comparing N output responses directly with their expected output responses for all said scan cells within said N clock domains and indicating errors immediately during the compare operation; and

(d) repeating the steps of (a)-(c) until a predetermined limiting criteria is reached, wherein (a) and (c) occur substantially concurrently.

44. The method of claim 43, wherein each said capture clock is programmable to contain one or more clock pulses for performing said shift/compare and capture operations on all said scan cells within one said clock domain; wherein said clock domain is solely controlled by said capture clock; and said capture clock can be either generated internally or controlled externally, and can operate either at its rated clock speed (at-speed) or at a selected clock speed.

45. The method of claim 43, further comprising providing N scan enable (SE) signals each within one said clock domain; wherein said SE signals are used to switch operations from shift/compact to capture, and vice versa; and further said SE signals can be generated internally or controlled externally, and are operated either at the rated clock speeds (at-speed) or at selected clock speeds.

46. The method of claim 45, wherein said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive said N scan enable (SE) signals; wherein said GSE signal is operated at a selected reduced clock speed.

47. The method of claim 43, wherein said generating and loading N predetermined stimuli further comprises operating all capture clocks at selected clock speeds or at the same clock speed, and when operated at the same clock speed, all said capture clocks are skewed so that at any given time only scan cells within one said clock domain are changing states to reduce power consumption.

48. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises performing said capture operation concurrently on a plurality of clock domains which do not have any logic block crossing each other.

49. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises applying said capture clocks in a selected order for detecting or locating additional faults in said integrated circuit or circuit assembly.

50. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises applying another ordered sequence of capture clocks selectively longer or shorter than said ordered sequence of capture clocks for detecting or locating additional faults in said integrated circuit or circuit assembly.

51. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises disabling one or more capture clocks to facilitate fault diagnosis.

52. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises selectively operating said capture clock at a selected clock speed for detecting or locating stuck-at faults within the clock domain controlled by said capture clock.

53. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises selectively operating said capture clock at its rated clock speed for detecting or locating delay faults within the clock domain controlled by said capture clock.

54. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises selectively reducing said capture clock speed to the level where delay faults associated with all multiple-cycle paths of equal cycle latency within the clock domain are tested at a predetermined rated clock speed.

55. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises selectively operating two said capture clocks at selected

clock speeds for detecting or locating stuck-at faults crossing two said clock domains.

56. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises selectively adjusting the relative clock delay of two said capture clocks operating at selected clock speeds for detecting or locating delay faults crossing two said clock domains.

57. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises selectively adjusting the relative clock delay of two said capture clocks to the level where delay faults associated with all multiple-cycle paths of equal cycle latency crossing two said clock domains are tested at a predetermined rated clock speed.

58. The method of claim 43, wherein said applying an ordered sequence of capture clocks further comprises controlling the relative clock delay between any two adjacent capture clocks internally or external to said integrated circuit or circuit assembly.

59. The method of claim 43, wherein said comparing N output responses directly with their expected output

responses further comprises selectively compacting said N output responses to signatures using a compact operation.

60. The method of claim 59, wherein said compacting N output responses to signatures further comprises comparing said signatures with their expected signatures after said predetermined limiting criteria is reached; wherein said comparing said signatures with their expected signatures further comprises comparing said signatures inside said integrated circuit or shifting out said signatures for comparison in an ATE.

61. The method of claim 43, wherein said scan cells are multiplexed D flip-flops or level sensitive latches, and further wherein said integrated circuit or circuit assembly under test is a full-scan or partial-scan design.

62. The method of claim 43, wherein said faults further comprise stuck-at faults and delay faults; wherein said stuck-at faults further comprises other stuck-type faults, such as open and bridging faults, and wherein said delay faults further comprises other non-stuck-type delay faults, such as transition (gate-delay), multiple-cycle delay, and path-delay faults.

63. An apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and

faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test mode, where N > 1 and each domain has a plurality of scan cells, said apparatus comprising:

(a) means for generating and loading N predetermined stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during the shift operation;

(b) means for applying an ordered sequence of capture clocks to all said scan cells within said N clock domains where one or more capture clocks must contain two or more clock pulses during the capture operation;

(c) means for comparing N output responses directly with their expected output responses for all said scan cells within said N clock domains and indicating errors immediately during the compare operation; and

(d) means for repeating the steps of (a)-(c) until a predetermined limiting criteria is reached, wherein (a) and (c) occur substantially concurrently.

64. The apparatus of claim 63, wherein said means of (a)-(d) are placed inside or external to said integrated circuit or circuit assembly.

65. A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or

circuit assembly in scan-test mode, where N > 1 and each domain has a plurality of scan cells, said method comprising the steps of:

(a) shifting in N predetermined stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during the shift-in operation;

(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains where one or more capture clocks must contain two or more clock pulses during the capture operation; and

(c) shifting out N output responses of all said scan cells for analysis during the shift-out operation.

66. The method of claim 65, further comprising providing N scan enable (SE) signals each within one said clock domain; wherein said SE signals are used to switch operations from shift/compact to capture, and vice versa; and further said SE signals can be generated internally or controlled externally, and are operated either at the rated clock speeds (at-speed) or at selected clock speeds.

67. The method of claim 66, wherein said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive said N scan enable (SE) signals; wherein said GSE signal is operated at a selected reduced clock speed.

68. The method of claim 65, wherein said applying an ordered sequence of capture clocks further comprises any means for generating the ordered capture sequence; wherein said ordered capture sequence does not include any shift clock pulses during said capture operation.

69. A computer-aided design (CAD) system for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test mode, where N > 1 and each domain has a plurality of scan cells, said CAD system comprising the computer-implemented steps of:

(a) compiling the HDL code or netlist that represents said integrated circuit or circuit assembly in physical form into a design database;

(b) performing scan rule check for checking whether said design database contains any multiple-capture scan rule violations;

(c) performing scan rule repair until all said multiple-capture scan rule violations have been fixed;

(d) performing multiple-capture scan synthesis for generating a scan HDL netlist; and

(e) generating HDL test benches and ATE test programs, where one or more capture clocks must

contain two or more clock pulses, for verifying the correctness of said scan HDL netlist.

70. The CAD system of claim 69, wherein said steps of (a)-(e) accept user-supplied scan control information and report the results and errors, if any.

71. The CAD system of claim 69, wherein said performing scan rule check further comprises determining the number of clock domains and capture clocks required for scan-test, the clock domains to be tested concurrently, the ordered sequence of capture clocks to be applied for scan-test, and the capture clocks to be operated at the rated clock speeds.

72. The CAD system of claim 69, wherein said performing multiple-capture scan synthesis further comprises inserting spare scan cells into selected clock domains.

73. The CAD system of claim 69, wherein said performing multiple-capture scan synthesis realizes said apparatus of claim 63 using said method of claim 43.

74. The CAD system of claim 69, wherein said generating HDL test benches and ATE test programs further comprises the steps of transforming said design database

into an equivalent combinational circuit model based on said ordered sequence of capture clocks, and performing combinational ATPG to generate the circuit's test patterns and report its fault coverage.

75. The CAD system of claim 69, wherein said generating HDL test benches and ATE test programs further comprises performing combinational logic simulation on said combinational circuit model to compute said circuit's signatures when a compact operation is employed to compact said circuit's output responses.